REMARKS

Applicants offer the above amendments and the following remarks in reply to the Office Action dated January 11, 2005 for the above-identified patent application.

In the Office Action, the Examiner objected to the specification for containing a reference that was not current for the parent application. In response, Applicant has amended the reference to include the patent number of the parent application. Applicant accordingly requests reconsideration and withdrawal of the objection to the specification.

The abstract was objected to as being too long. In response, Applicant is providing a replacement abstract with fewer than 150 words. In view of the above amendment, Applicant requests reconsideration and withdrawal of the objection to the abstract.

Claims 12-24 were pending in the above-identified application when last examined and are amended as indicated above. The claim amendments clarify the claim language and are not intended to limit the scope of the claims, unless the claim language is expressly quoted in the following remarks to distinguish over the art cited.

Claims 12-15 and 18-24 were rejected under 35 U.S.C. § 103(a) as unpatentable over U.S. Pat. No. 5,585,436 (Ooishi) in view of U.S. Pat. No. 6,088,264 (Hazen). Applicants respectfully traverse the rejection.

Independent claim 12 distinguishes over the combination of Ooishi and Hazen at least by reciting, "A Flash memory comprising: a plurality of array planes that constitute all storage corresponding to a logical address space of the Flash memory, each array plane including a plurality of blocks of memory cells, wherein the blocks store parameters, code, and data, and all of the blocks in the array planes have a uniform size selected for parameter storage."

Ooishi and Hazen fail to disclose or suggest a Flash memory storing parameters, code, and data in blocks having a uniform size selected for parameter storage. In particular, Ooishi fails to mention Flash memory. Hazen is directed to Flash memory but fails to disclose or suggest use of blocks sized for parameter storage to store code and data. Accordingly, Ooishi and Hazen whether considered separately or in combination fail to suggest a Flash memory

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storing parameters, code, and data in blocks having a uniform size selected for parameter storage.

Further, it would not have been obvious to employ the redundancy system of Ooishi in a Flash memory storing parameters, data, and code such as in specific embodiments disclosed by Hazen because conventional Flash memory storing parameters, code, and data have had blocks of different sizes. In particular, Ooishi and Hazen fail to suggest how use of a content addressable memory to identify block addresses corresponding to defective blocks could adapt to blocks of varying sizes. In accordance with an aspect of Applicant's invention, a Flash memory uses uniform block size for parameters, code, and data, which facilitates use of a block redundancy and repair system. However, Ooishi and Hazen fail to suggest such a combination. Claim 12 is therefore patentable over the combination of Ooishi and Hazen.

Claims 13 and 14 depend from claim 12 and are patentable over the combination of Ooishi and Hazen for at least the same reasons that claim 12 is patentable over the combination.

Independent claim 18 distinguishes over the combination of Ooishi and Hazen at least by reciting, "storing parameters, code, and data in separate blocks of memory cells, wherein each of the blocks has a uniform size selected for parameter storage." As noted above, Ooishi and Hazen fail to disclose or suggest storing parameter, code, and data in blocks sized for parameter storage. Accordingly, claim 18 is patentable over the combination of Ooishi and Hazen.

Claims 19-24 depend from claim 18 and are patentable over the combination of Ooishi and Hazen for at least the same reasons that claim 18 is patentable over Ooishi and Hazen.

For the above reasons, Applicant requests reconsideration and withdrawal of this rejection under 35 U.S.C. § 103.

Claims 16 and 17 were rejected under 35 U.S.C. § 103(a) as unpatentable over Ooishi in view of Hazen and further in view of U.S. Pat. No. 6,233,181 (Hidaka) and U.S. Pat. No. 6,665,221 (Abedifard). Applicant respectfully traverses the rejection.

Claims 16 and 17 depend from claim 12, which is patentable over Ooishi and Hazen for at least the reasons given above. In particular, Ooishi and Hazen fail to disclose or suggest a Flash memory storing parameters, code, and data in blocks having a uniform size selected for parameter storage. The Examiner cites Hidaka for teaching array planes having at least one spare memory element and Abedifard for teaching a spare global bit line that connects to

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all blocks in an array plane. However, such teachings do not affect the above showing that claim 12 is patentable. Accordingly, claims 16 and 17 are patentable over the combination of Ooishi, Hazen, Hidaka, and Abedifard at least because the combination fails to suggest "A Flash memory comprising: a plurality of array planes that constitute all storage corresponding to a logical address space of the Flash memory, each array plane including a plurality of blocks of memory cells, wherein the blocks store parameters, code, and data, and all of the blocks in the array planes have a uniform size selected for parameter storage," as recited in claim 1.

For the above reasons, Applicants request reconsideration and withdrawal of this rejection under 35 U.S.C. § 103.

In summary, claims 12-24 were pending in the application. This response amends claims 12-14, 16, and 18. For the above reasons, Applicants respectfully request allowance of the application including claims 12-24.

Please contact the undersigned attorney at (408) 927-6700 if there are any questions concerning the application or this document.

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Respectfully submitted,

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